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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,309	03/22/2004	Junichiro Kobayashi	SON-2977	9147

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/805,309	KOBAYASHI, JUNICHIRO	
	Examiner	Art Unit	
	Thao X. Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,13-15 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,13-15 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 14 Feb. 2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3,5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over by FR 2726125 to Delage et al. in view of US 6680791 to Demir et al.

Regarding claim 1, Delage discloses a semiconductor device in fig. 5b comprising: a semiconductor mesa portion (E/cb/B/C) formed on a substrate S, fig. 4, including a stack of at least a collector layer C, a base layer B (below layer c_b), and an emitter layer E formed in narrower region compared with said base layer B, fig. 5b, and

functioning as an active region of a bipolar transistor; a base contact pad mesa portion R_B, fig. 5b, formed on said substrate S apart from said semiconductor mesa portion and formed with a height the same as the height of the top surface of said base layer B, fig. 5b; and a conductive layer (Pont-air), formed integrally with a base electrode (left portion of Pont-a-air) formed connected to said base layer B at part of a region of formation of said base layer B other than the region of formation of said emitter layer E, fig. 5b, a base contact pad electrode (right portion of Pont-a-air) formed above said base contact pad mesa portion R_B in a region other than near the edges of the top surface of said base contact pad mesa portion R_B, fig. 5b, and an interconnect (middle portion of Pont-a-air) for connecting said base electrode and said base contact pad electrode.

But Delage does not discloses the semiconductor device wherein an insulating film is formed below said conductive layer between said semiconductor mesa portion and said base contact pad mesa portion.

However, Demir discloses the semiconductor device in fig. 5 wherein an insulating film 332, col. 14 line 26, comprising low dielectric material or even air, col. 14 line 44, is formed below said conductive layer 330, col. 14 line 25, between said semiconductor mesa portion 316 and said base contact pad mesa portion 322, fig. 5. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the insulating layer 332 teaching of Demir with Delage's device, because it would have ensured a low capacitance of the bridge connection as taught by Demir in col. 14 lines 40-45. Furthermore,

at the time of the invention was made; it would have been obvious to one of ordinary skill in the art to use the dielectric material teaching of Demir to fill the air gap structure of Delage, because such material substitution would have been considered a mere substitution of art-recognized equivalent values, MPEP 2144.06.

Regarding claim 2, Delage discloses a semiconductor device wherein the surface layer of said base contact pad mesa portion is formed by the same layer as said base layer, fig. 5b.

Regarding claims 3 and 5, Delage discloses a semiconductor device wherein the area under said conductive layer between said semiconductor mesa portion and said base contact pad mesa portion forms a space, fig. 5b, and wherein said base electrode is formed in a region other than the region of formation of said emitter layer and other than near the edges of said base layer, fig. 5b.

Regarding claim 17, Delage discloses the semiconductor device as set forth in claim 1, wherein said semiconductor mesa portion is comprised of a stack of a compound semiconductor and has a heterojunction bipolar transistor, fig. 5b

4. Claims 13-15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by FR 2726125 to Delage et al.

Regarding claim 13, Delage discloses a semiconductor device in fig. 5b comprising: a semiconductor mesa portion (where emitter E is located) formed on a substrate including a stack of at least a collector layer (right above sous-collecteur), fig. 5b, a base layer (below layer cb), and an emitter layer E formed in narrower region

compared with said base layer, fig. 5b, and functioning as an active region of a bipolar transistor; a base contact pad mesa portion R_B formed on said substrate apart from said semiconductor mesa portion (where E is located), fig. 1B, and formed with a height the same as the height of the top surface of said base layer, fig. 5b; and a conductive layer (Pont-a-air), fig. 5b, formed integrally with a base electrode (left portion of Pont-a-air in contact with base) formed connected to said base layer at part of a region of formation of said base layer other than the region of formation of said emitter layer E, fig. 5b, a base contact pad electrode (right portion of Pont-a-air in contact with R_B) formed above said base contact pad mesa portion in a region other than near the edges of the top surface of said base contact pad mesa portion, fig. 5b, and an interconnect (middle portion of Pont-a-air) for connecting said base electrode and said base contact pad electrode, wherein said base electrode is formed in a region other than the region of formation of said emitter layer and other that near edges of said base layer, fig. 5b.

But Delage does not disclose the semiconductor device wherein a distance between said semiconductor mesa portion and said base contact pad mesa portion is 1 to 5 micron. However, Delage discloses a general distance or a gap between said semiconductor mesa portion and said base contact pad mesa portion R_B, fig. 5b. Accordingly, it would have been obvious to one of ordinary skill in art to use general gap teaching of Delage in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable

range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 14, Delage discloses a semiconductor device as set forth in claim 13, wherein the surface layer of said base contact pad mesa portion is formed by the same layer as said base layer, fig. 5b.

Regarding claim 15, Delage discloses a semiconductor device as set forth in claim 13, wherein the area under said conductive layer between said semiconductor mesa portion and said base contact pad mesa portion forms a space, fig. 5b.

Regarding claim 17, Delage discloses the semiconductor device as set forth in claim 1, wherein said semiconductor mesa portion is comprised of a stack of a compound semiconductor and has a heterojunction bipolar transistor, fig. 5b

Response to Arguments

5. Applicant's arguments with respect to claims 1-3,5-7 have been considered but are moot in view of the new ground(s) of rejection.

6. With respect to claims 13-14 and 17, since the applicant has not established the criticality of space distance stated. Where patentability is said to be based upon particular chosen dimension or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
08 March 2006